

Abu Asaduzzaman | Research Statement

My current research focus includes high performance computer/computing (HPC) systems, machine learning (ML), HPC and ML in healthcare technology, and performance and power evaluation. I have been conducting innovative research to develop power aware HPC systems since I was a PhD student at Florida Atlantic University (FAU). As a principle investigator (PI) at Wichita State University (WSU), I

have received several research grants from the WSU internal sources. I have refereed journal articles, book chapters, more than 50 peer reviewed and more than ten technical articles out of my research work. I have been serving the community as a panel reviewer, panel presenter, invited speaker, journal reviewer, technical/international program committee member, and numerous volunteer at my university.

At the Center for Architecture and Parallel Programming Laboratory (CAPPLab) at WSU, I have been leading several grant research projects. In the project funded by ANL (08/2020-08/2023), we are working on Exascale machines using the Portable, Extensible Toolkit for Scientific Computing (PETSc) and the Data Management Network (DMNetwork) libraries that are of interest to generate realistic traffic data in Hierarchical Data Format 5 (HDF5) for selected applications. We are also working on netconvert (a network simulator) and develop/update PETSc subroutines for data processing. The resulting code development is included into the PETSc distribution benefiting the scientific community in large. In the project funded by DOE Visiting Scientist Program at Lawrence Berkeley National Laboratory (LBNL) (06/2020-08/2021), we are working on the generation through a feasible methodology for generating graphic design system files of matrix multiplication (MMM). We synthesized the Pythonic code in large.

During my undergraduate study at Bangladesh University of Engineering and Technology (BUET), an ABET accredited institution. I developed a methodology for the design of Computer Aided Design of Integrated Circuits (CADIC) using Verilog. This research work was accepted in partial fulfillment of the requirements for the M.Sc. degree in Computer Engineering at FAU.

My research interests include cache coherent multiprocessor systems with a distributed shared memory architecture which is a variation of the Cache Consistent Shared Memory (CCSHM) architecture. In this architecture, snoopy cache coherence protocol is used. The number of processors per cluster is small. Clusters are

